JYOTI NIVAS COLLEGE AUTONOMOUS
SYLLABUS FOR 2021 BATCH AND THEREAFTER
PROGRAMME: BCA
SEMESTER:II -COMPUTER ARCHITECTURE

COURSE CREDITS: 03 **NO. OF HOURS: 45**

COURSE OUTCOMES (COS):

1.Conceptualize the basic model of a computer and it's various instructions.

2.Analyse the different instruction formats and addressing modes.

3.Define different number systems, register transfer logic and arithmetic operations.

4.Analyse memory management system.

UNITI **12**

Hours

NumberSystems: Binary,Octal,Hexadecimalnumbers,baseconversion,addition,subtraction of binary numbers, one's and two's complements, positive and negative numbers,charactercodesASCII,EBCDIC.**ComputerArithmetic:**AdditionandSubtraction, MultiplicationandDivisionalgorithms,Floating-pointArithmeticOperations,Decimalarithmetic operations. **Structure of Computers:** Computer types, Functional units, Basicoperational concepts, Von-Neumann Architecture, Bus Structures, Software, Performance,Multiprocessors and Multicomputer, **Digital Logic Circuits:** Logic gates, Boolean algebra,Map Simplification. Combinational Circuits: Half Adder, Full Adder, flip flops. **Sequentialcircuits:**Shift registers, Counters, Integrated Circuits, Mux, Demux, Encoder,Decoder.**Datarepresentation:**Fixed and Floatingpoint.

UNITII **11**

Hours

BasicComputerOrganizationandDesign: Instructioncodes,ComputerRegisters,ComputerInstructionsandInstructioncycle.TimingandControl,Memory-ReferenceInstructions,Input-Outputandinterrupt.**Centralprocessingunit:**Stackorganization,InstructionFormats,AddressingModes,DataTransferandManipulation,ComplexInstructionSetComputer(CISC)Reduced InstructionSetComputer(RISC),CISCvsRISC

UNITIII **11**

Hours

Register Transfer and Micro-operations: Register Transfer Language, Register Transfer,Bus and Memory Transfers, Arithmetic Micro-Operations, Logic Micro-Operations, ShiftMicro-Operations, Arithmetic logic shift unit. Micro-programmed Control: Control Memory,Address Sequencing, Micro-Program example, **Design of Control Unit. Input Output:** I/Ointerface, Programmed IO, Memory Mapped IO, Interrupt Driven IO, DMA. **Instructionlevelparallelism:**Instructionlevelparallelism(ILP)-overcomingdatahazards,limitationsofILP

UNIT-IV **11**

Hours

MemorySystem: MemoryHierarchy,SemiconductorMemories,RAM(RandomAccessMemory),ReadOnlyMemory(ROM),TypesofROM,CacheMemory,Performanceconsiderations, Virtual memory, Paging, Secondary Storage, RAID. **Multiprocessors AndThread level Parallelism:** Characteristics of multiprocessors, Multi-Threaded Architecture,DistributedMemory MIMDArchitectures,Interconnection structures.

TextBooks:

1. ManoMMorris,"ComputerSystem Architecture", 3rdEdition PearsonIndia(2019).
2. William Stallings, "Computer Organization and Architecture designing forperformance",10thedition,Pearson(2016)

ReferenceBooks:

1. SubrataGhoshal,"ComputerArchitectureAndOrganization",PearsonIndia(2011).
2. AndrewS.Tanenbaum"StructuredComputerOrganization",5thedition, PearsonEducation Inc(2006).
3. CarlHamacher,ZvonksVranesic,SafeaZaky,"ComputerArchitectureAndOrganization",5theditionMcGrawHillNewDelhi,India(2002).
4. Kai Hwang, "Advanced Computer Architecture - Parallelism, Scalability,Programmability", TataMcgraw-Hill(2008).